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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,144	08/27/2004	Douglas D. Coolbaugh	BUR920040107US1	5143

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,144	COOLBAUGH ET AL.	
	Examiner	Art Unit	
	KHIEM D. NGUYEN	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-9 and 12-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-9 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6-9 and 12-14 rejected under 35 U.S.C. 102(b) as being anticipated by Coolbaugh et al. (U.S. Pub. 2003/0122128).

In re claim 1, **Coolbaugh** discloses a varactor structure comprising: a semiconductor substrate **10** of a first conductivity type, the substrate **10** including a subcollector **12** of a second conductivity type (see page 2, paragraph [0038]) located below an upper region of the substrate **10**, the first conductivity type is different from the second conductivity type; a well region located in the upper region of the substrate **10**, wherein the well region includes outer well regions **22** of the second conductivity type and an inner well region **18** of the first conductivity type, each well of alternating conductivity type of the well region is separated at an upper surface by an isolation region **16** (see page 2, paragraph [0037] to page 3 paragraph [0043] and FIGS. 1-5) and each outer well region **22** has an upper surface which includes a source/drain region (see page 3, paragraph [0043]); and

a field effect transistor having at least a gate conductor **54** of the first conductivity type located above the inner well region **18** (see page 3, paragraph [0047] to page 4, paragraph [0050] and FIGS. 6-10); and

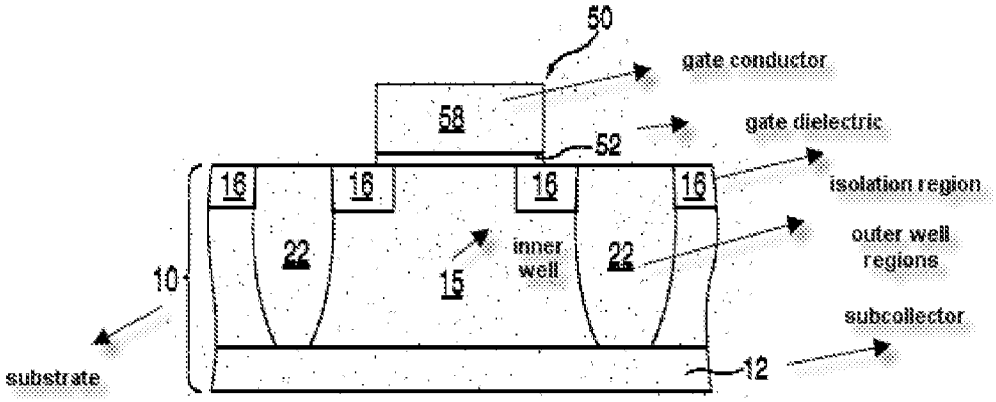

FIG. 10

wherein, the outer well regions **22** and the inner well region 46 are in contact with the subcollector **12** having the second conductivity type (see page 3, paragraph [0043]), wherein said each well of alternating conductivity type of said well region extends beneath the isolation region to the subcollector **12** such that neighboring well regions **18, 22** are in contact with each other along an entire depth of each well region, wherein the subcollector **12** continuously extends through the outer well region **22** and the inner well region **18** of the substrate (see FIGS. 5 and 10 and related text).

In re claim 2, as applied to claim 1 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the first conductivity type comprises a p-type dopant and second conductivity type comprises a n-type dopant (see page 2, paragraphs [0038]-[0041]).

In re claim 3, as applied to claim 1 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the first conductivity type comprises a n-type dopant and the second conductivity type comprises a p-type dopant (see page 2, paragraphs [0038]-[0041])).

In re claim 6, as applied to claim 1 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the upper region of the substrate **10** comprises an epitaxial semiconductor layer (optional epi Si layer, not shown) (see page 2, paragraph [0039]).

In re claim 7, as applied to claim 1 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the field effect transistor further comprises a gate dielectric **52** located beneath the gate conductor **54**, a hard mask **56** located on the gate conductor **54**, at least one spacer located on sidewalls of the gate conductor **54** and abutting source/drain regions (see page 3, paragraph [0059] to page 4, paragraph [0050] and FIG. 9).

In re claim 8, as applied to claim 1 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the gate conductor **54** comprises polysilicon (see page 3, paragraph [0049]).

In re claim 9, **Coolbaugh** discloses a varactor structure comprising a p-type semiconductor substrate **10**, the p-type substrate including an n-type subcollector **12** located below an upper region (see page 2, paragraph [0038]) of the substrate **10**; a well region located in the upper region of the substrate **10**, wherein the well region includes outer N-well regions **22** and an inner P-well

region **18**, each well of alternating conductivity type of the well region is separated at an upper surface by an isolation region **16** (see page 2, paragraph [0037] to page 3, paragraph [0043] and FIGS. 1-5) and each outer well region **22** has an upper surface which includes a source/drain region (see page 3, paragraph [0043]); and a field effect transistor having at least a p-type gate conductor **54** located above the inner P-well region **18**, the outer N-well regions **22** and the inner P-well region **18** are in contact with the n-type subcollector **12** (see page 3, paragraph [0047] to page 4, paragraph [0050] and FIGS. 6-10),

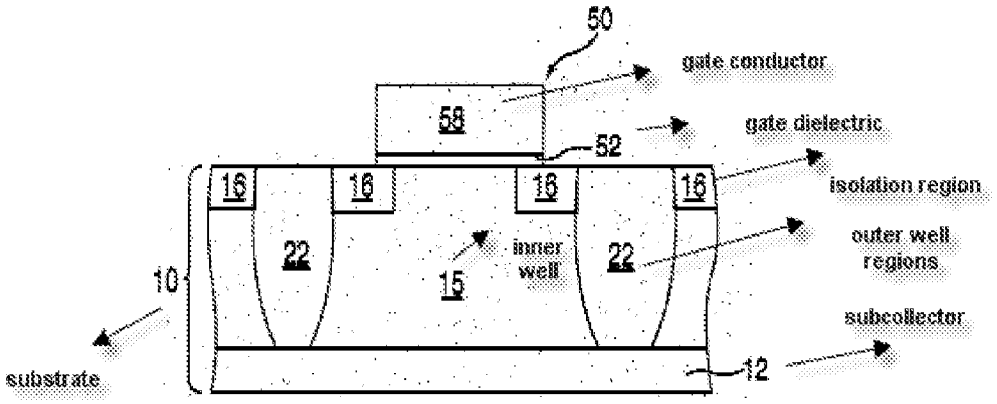

FIG. 10

wherein the outer N-well regions **22** and the inner P-well region **18** extend beneath the isolation region **16** to the n-type subcollector such that neighboring well regions **18, 22** are in contact with each other along an entire depth of each well region, wherein the n-type subcollector **12** continuously extends through the outer N-well regions **22** and the inner P-well region **18** (see FIGS. 5 and 10 and related text).

In re claim 12, as applied to claim 9 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the upper region of the substrate **10** comprises an epitaxial semiconductor layer (optional epi Si layer, not shown) (see page 2, paragraph [0039]).

In re claim 13, as applied to claim 9 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein field effect transistor further comprises a gate dielectric **52** located beneath the gate conductor **54**, a hard mask **56** located on the gate conductor **54**, at least one spacer located on sidewalls of the gate conductor **54** and abutting source/drain regions (see page 3, paragraph [0059] to page 4, paragraph [0050] and FIG. 9).

In re claim 14, as applied to claim 9 above, **Coolbaugh** discloses all claimed limitations including the limitation wherein the gate conductor **54** comprises polysilicon (see page 3, paragraph [0049]).

Response to Applicants' Amendment and Arguments

3. Applicants' arguments with respect to claims 1-3, 6-9 and 12-14 have been considered but are moot in view of the new ground(s) of rejection necessitated by the amendment filed on April 09th, 2008.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to

expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brook Kebede/
Primary Examiner, Art Unit 2823

/Khiem D. Nguyen/
Examiner, Art Unit 2823